CLAIMS

What is claimed is:

1. A method for erasing a bit of a memory cell in a non-volatile memory cell array, the method comprising:

applying an erase pulse to at least one bit of at least one memory cell of said array;

waiting a delay period wherein a threshold voltage of said at least one memory cell drifts to a different magnitude than at the start of the delay period; and

after said delay period, erase verifying said at least one bit to determine if said at least one bit is less than a reference voltage level.

2. The method according to claim 1, wherein said delay period is determined as a function of prior threshold voltage drift behavior of at least one similar memory cell.

3. The method according to claim 1, wherein during said delay period, an environmental condition of said at least one memory cell remains generally unchanged.

4. The method according to claim 1, further comprising changing an environmental condition of said at least one memory cell during said delay period.

5. The method according to claim 1, wherein said environmental condition comprises at least one of temperature, pressure, and humidity.

6. The method according to claim 1, wherein an erase condition used to erase said at least one memory cell remains generally unchanged throughout said delay period.

7. The method according to claim 1, further comprising changing an erase condition used to erase said at least one memory cell after said delay period has started.

8. The method according to claim 1, wherein said erase condition comprises at least one of a gate voltage, a drain voltage, a source voltage, and a time duration of an erase pulse.

9. The method according to claim 1, wherein said at least one memory cell comprises a channel formed in a substrate, two diffusion areas formed one on either side of said channel in said substrate, and an oxide-nitride-oxide (ONO) layer formed at least over said channel, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers, and wherein said delay period is determined as a function of the thickness of said bottom layer.

10. The method according to claim 1, wherein if a threshold voltage of said at least one bit is not less than said reference voltage level, at least one more erase pulse is applied to said at least one bit.

11. The method according to claim 1, wherein if a threshold voltage of said at least one bit is less than said reference voltage level, at least one more erase pulse is applied to said at least one bit.

12. A non-volatile memory cell array comprising:

a plurality of memory cells;

a power supply adapted to generate erase pulses to bits of said cells; and

a controller in communication with said power supply, said controller adapted to perform the steps of:

applying an erase pulse to at least one bit of at least one memory cell of said array;

waiting a delay period wherein a threshold voltage of said at least one memory cell drifts to a different magnitude than at the start of the delay period; and

after said delay period, erase verifying said at least one bit to determine if said at least one bit is less than a reference voltage level.

13. The array according to claim 12, wherein said memory cells comprise nitride read only memory (NROM) cells.